Fabrication of 4H-Silicon Carbide BAW Gyroscopes

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Abstract

Bulk acoustic wave (BAW) gyroscopes fabricated from 4H-silicon carbide (4H-SiC) enable unprecedented performance in inertial navigation systems due to the material's exceptional mechanical properties and low intrinsic phonon dissipation. Unlike silicon-based devices, 4H-SiC offers superior thermal conductivity, transverse isotropy, and higher quality (Q) factors, making it ideal for harsh-environment applications. This work details a wafer-scale fabrication process for 4H-SiC BAW gyroscopes, beginning with chromium/gold seed layer deposition and nickel electroplating to form an etch mask, followed by high-aspect-ratio deep reactive ion etching to create capacitive transduction gaps with sub-200nm sidewall roughness. The resulting devices demonstrate Q-factors exceeding 5 million at 3MHz, enabled by precise control of etch profiles and minimization of thermoelastic damping. By overcoming key challenges in 4H-SiC microfabrication, including sidewall roughness and etch uniformity, this process establishes a foundation for manufacturing high-performance MEMS gyroscopes that surpass the limitations of conventional silicon technology.

Introduction

The demand for high-precision inertial sensors has grown significantly with advancements in autonomous navigation, aerospace systems, and wearable technologies. Bulk acoustic wave (BAW) gyroscopes, which rely on the resonant vibration of microstructures to detect angular rotation, have emerged as a promising solution due to their potential for ultra-high sensitivity and stability. However, conventional silicon-based MEMS gyroscopes face fundamental limitations imposed by material properties, particularly phonon-induced energy dissipation that restrict their quality (Q) factors and overall performance in harsh environments.

4H-silicon carbide (4H-SiC) has gained attention as a superior alternative to silicon for MEMS resonators, offering exceptional mechanical stiffness, thermal conductivity, and chemical stability. Its hexagonal crystal structure provides transverse isotropy, enabling degenerate resonant modes critical for gyroscopic operation, while its low Akhiezer dissipation allows Q-factors orders of magnitude higher than those achievable in

silicon. Despite these advantages, the widespread adoption of 4H-SiC in MEMS has been hindered by fabrication challenges, particularly in achieving high-aspect-ratio structures with smooth sidewalls necessary for capacitive transduction.

This paper presents a comprehensive fabrication methodology for 4H-SiC BAW gyroscopes, addressing critical process steps from seed layer deposition to deep reactive ion etching (DRIE). We demonstrate how optimized nickel hard masking and etch parameters enable the realization of high-Q resonators with 200nm sidewall roughness, while also examining the impact of crystal orientation and temperature-dependent performance. The resulting devices achieve Q-factors exceeding 5 million at 3MHz, representing a significant advancement in MEMS gyroscope technology. By establishing a reliable wafer-scale process, this work paves the way for the integration of 4H-SiC inertial sensors in applications where silicon-based devices fall short, including high-temperature aerospace systems and precision navigation platforms.

By systematically investigating critical parameters such as mask adhesion, etch chemistry, and sidewall passivation, this approach enables the realization of high-Q resonators with 200nm sidewall roughness. The resulting devices demonstrate exceptional performance characteristics, including Q-factors exceeding 5 million at 3MHz and improved temperature stability compared to silicon-based counterparts. These advancements establish a foundation for next-generation inertial sensors capable of operating in demanding environments where conventional MEMS technologies prove inadequate.

Fabrication Flow

Seed Layer Deposition

The process begins with the deposition of a metallic seed layer onto a 4H-SiC wafer. An e-beam evaporator is employed to sequentially deposit a 20 nm chromium layer, which promotes adhesion, followed by a 100 nm gold layer to ensure electrical conductivity. The e-beam evaporator operates by generating a focused electron beam that vaporizes the target material (chromium or gold) in a high-vacuum environment, allowing for precise and contamination-free deposition.

Figure 1. Not-to-scale representation of the SiC wafer with a 20 nm chromium adhesive layer, followed by the 100 nm gold layer on top.

Photolithography & Pattern Transfer

Photolithography is used to define the gyroscope's structural patterns. The wafer is coated with AZ-10XT photoresist using a spin coater, which rotates the wafer at high speeds (500 rpm for 5 seconds, followed by 1400 rpm for 40 seconds) to achieve a uniform layer. A soft bake at 110°C for 3 minutes solidifies the resist.

The pattern is then transferred using a maskless aligner, which projects ultraviolet light (λ = 375 nm) through a digital micromirror device (DMD) to selectively expose the photoresist. The maskless aligner offers flexibility in pattern design, as the DMD

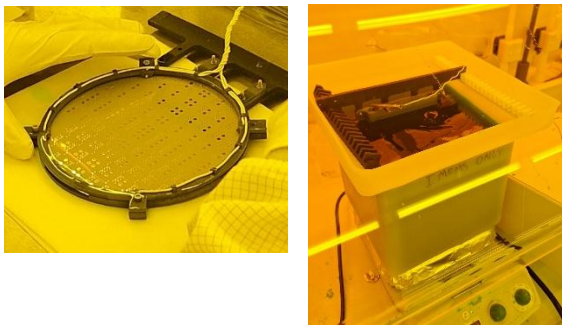
dynamically adjusts the exposure pattern without the need for physical masks. An inverted exposure strategy is employed, where the UV light exposes all areas except the intended pattern, facilitating subsequent electroplating for the nickel mask.

Figure 2. Not-to-scale representation of SiC wafer after pattern is developed.

Nickel Mask

The exposed gold regions serve as a conductive base for electroplating a nickel mask. During electroplating, the wafer acts as the cathode, while a nickel anode is immersed in an electrolyte solution. A direct current is applied, causing nickel ions to deposit onto the gold surface. The resulting nickel mask, approximately 8.5 µm thick, exhibits exceptional resistance to reactive ion etching (RIE) gases, ensuring pattern integrity during subsequent steps. After nickel has been successfully deposited, photoresist is removed using acetone or a piranha solution, which is a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) in a 3:1 ratio.

a) b)



c) d)

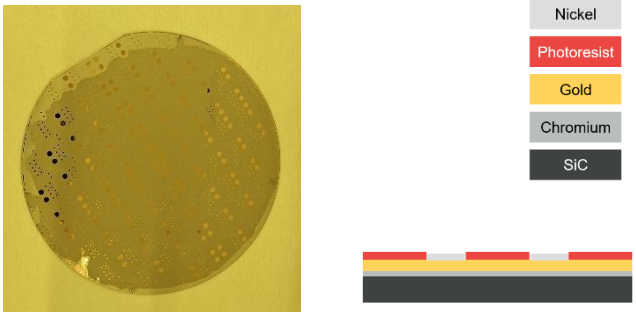


Figure 3. a) SiC wafer is secured in a wafer holder for electroplating. b) SiC wafer and nickel bar are suspended in solution while electroplating. c) SiC wafer after nickel electroplating. d) Not-to-scale representation of SiC wafer after nickel has been deposited.

Deep Reactive Ion Etching (DRIE)

The SiC wafer is etched using two specialized systems: the Vision RIE and the Versaline ICP. The Vision RIE, a reactive ion etcher, first removes the exposed gold and chromium seed layer. This system generates a plasma of reactive gases (e.g., SF_6), which chemically and physically bombard the wafer surface, selectively etching the unprotected regions.

For the bulk SiC etching, the Versaline ICP (inductively coupled plasma) etcher is employed. The ICP system produces a high-density plasma by coupling radiofrequency energy into a gas mixture, enabling deep and anisotropic etching. Temperature plays a critical role in this process. Experimental trials revealed that maintaining the wafer at 10°C yields optimal results, with minimal pothole formation and uniform etching. Higher temperatures (e.g., 40°C) lead to thermal stress, causing mask degradation and wafer warping.

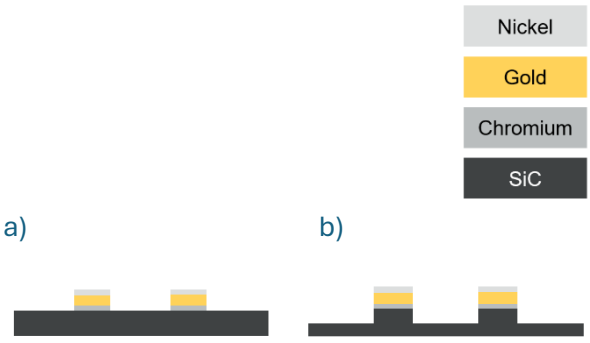


Figure 4. a) Seed layer is etched with Vision RIE. b) SiC is etched with Versaline ICP.

Seed Layer & Mask Removal

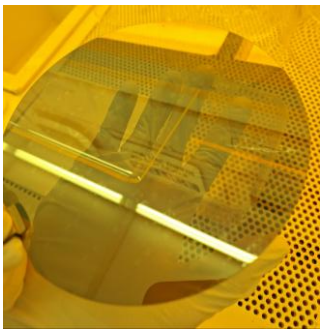
The first step involves a thorough cleaning of the wafer using a piranha solution. This solution is heated to approximately 80°C and is used to remove organic residues and other contaminants from the wafer surface. The piranha treatment is typically performed for 10 minutes or until the chemical reaction is finished, after which the wafer is rinsed with deionized (DI) water to neutralize any remaining acid.

The nickel mask, which served as a protective layer during etching, is now removed as well. A solution of nitric acid (HNO_3) and hydrogen peroxide (H_2O_2) in a 3:1 ratio is prepared and heated to 80°C on a hotplate. The wafer is immersed in this solution until the nickel layer is completely dissolved. During this process, the nickel reacts with the nitric acid, forming nickel nitrate and releasing nitrogen oxides, which appear as bubbles. The progress of the reaction can be monitored visually, as the disappearance of the metallic nickel indicates completion. The wafer is once again rinsed after the process is complete.

Next, the gold seed layer is removed using a mixture of hydrochloric acid (HCl) and nitric acid (HNO_3) in a 3:1 ratio, also heated to 80°C. As the gold layer reacts with the acids, the solution becomes a characteristic orange color, signaling the dissolution of gold as well as residual photoresist. The wafer is rinsed with DI water

The final step in the post-etch cleaning process is the removal of the chromium adhesion layer. A specialized chromium etchant is used for this purpose. Unlike the previous steps, this process does not require heating. The wafer is immersed in the etchant at room temperature until the chromium layer is fully dissolved. The progress can be observed as the chromium dissolves, leaving behind a clean, transparent 4H-SiC surface. Once the etching is complete, the wafer is thoroughly rinsed with DI water to remove any residual chemicals.

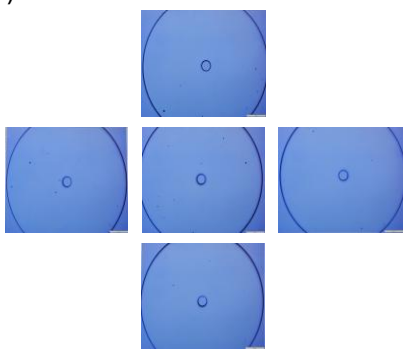
a)



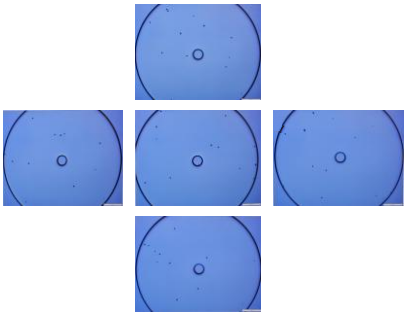
b)

Figure 5. a) SiC wafer that has been stripped of seed layer and nickel mask. Note the wafer is transparent once again. b) Cavities of the wafer can be seen up close from the etching process.

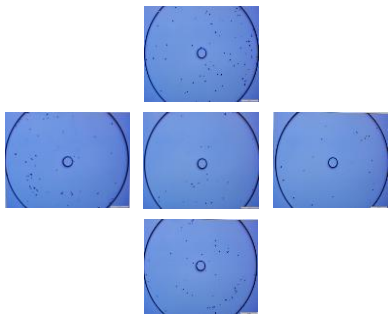
a) 10°C



b) 20°C



c) 40°C



d) 60°C

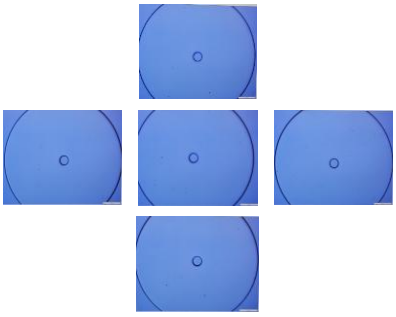


Figure 6. Note: Originally, there was a fifth wafer, 30°C. It was damaged during the etching process and had to be discarded. a) 10°C: Wafer has small and few potholes. b) 20°C: Wafer exhibits more, larger potholes. c) 40°C: Wafer has numerous, large potholes. d) 60°C: Wafer exhibits very few and very small potholes.

TEOS Deposition and Annealing (Five Iterations)

Tetraethyl orthosilicate (TEOS) deposits a silicon dioxide (SiO_2) layer that serves as an electrical insulator. During low-pressure chemical vapor deposition (LPCVD), TEOS vapor decomposes at high temperatures to form a uniform SiO_2 film, isolating conductive components while passivating the SiC surface. Each ~0.8 µm deposition cycle is followed by annealing to densify the oxide and minimize stress. Silicon carrier wafers are interleaved with the transparent SiC wafers during deposition; not only to enable reflectometer-based thickness measurements (impossible on optically clear SiC) but also to improve deposition uniformity by stabilizing gas flow dynamics and thermal gradients across the batch.